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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,536	10/31/2001	Pradeep Sindhu	1014-014US01	4412

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EXAMINER	
AVELLINO, JOSEPH E	
ART UNIT	**PAPER NUMBER**
2143	

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/004,536	SINDHU ET AL.	
	Examiner	Art Unit	
	Joseph E. Avellino	2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-32,34 and 35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-32,34 and 35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9, 11-33, and 34-35 are presented for examination; claims 1, 9, 18, 24, 30, and 35 independent. The Office acknowledges the cancellation of claims 10 and 33.

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-9, 11-33, 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mathur (USPN 6,424,658) in view of Muller et al. (USPN 6,246,680) (hereinafter Muller)

3. Referring to independent claim 1, Mathur discloses a routing component 22, 24 comprising:

a first interface to communicate with a first network interface (Figure 3, ref. 32, 34);

a second interface to communicate with a second network interface, wherein the first interface and the second interface are integrated within a single integrated circuit (i.e. network switch chip) (Figure 3, ref. 36, 38; col. 3, lines 55-60); and

an embedded memory (i.e. FIFO) within the integrated circuit to buffer data communicated in a first direction from the first interface to the second interface (Figure 3, ref. 32, 34).

Mathur does not specifically disclose a memory interface to couple the integrated circuit to an external memory for buffering data communicated in a second direction from the second interface to the first interface. In analogous art, Muller discloses another routing component which includes a memory interface 220 to couple the element to an external memory for buffering data communicated from the second interface to the first interface (col. 4, line 61 to col. 5, line 4). It would have been obvious to one of ordinary skill in the art to combine the teaching of Muller with Mathur to provide a buffered architecture to Mathur to provide temporary storage for efficient allocation of per port buffering that is proportional to the amount of traffic through a given port as supported by Muller (col. 8, lines 35-40).

4. Referring to claim 2, Mathur discloses a first control unit to buffer in the embedded memory data that is received from the first interface and forwarded to the second interface (e.g. abstract). Mathur does not disclose a second control unit to buffer in the external memory data that is received from the second interface and forwarding to the first interface. In analogous art, Muller discloses another routing component which includes a second control unit 220 to buffer in the external memory data that is received from the second interface and forwarding to the first interface (col. 7, line 35 to col. 8, line 35). It would have been obvious to one of ordinary skill in the art

to combine the teaching of Muller with Mathur to provide a buffered architecture to Mathur to provide temporary storage for efficient allocation of per port buffering that is proportional to the amount of traffic through a given port as supported by Muller (col. 8, lines 35-40).

5. Referring to claim 3, Mathur in view of Muller disclose the system substantively as described in claim 2. Mathur in view of Muller do not specifically disclose the external memory has a greater storage capacity than the embedded memory, however it is well known that external memory (i.e. hard drives, flash drives, etc.) can have a higher storage capacity than embedded memory such as registers and Random Access Memory. Therefore it would have been obvious to assume the external memory would have a greater storage capacity than the embedded memory since it would allow for more packets to be stored and thereby reducing page faults in the external device.

6. Referring to claim 4, Mathur discloses the first interface comprises a WAN (i.e. network) interface (col. 6, lines 3-15).

7. Referring to claim 5, Mathur discloses the second interface comprises a switch fabric interface (i.e. token ring) (Figure 3, ref. 30, 42).

8. Referring to claim 6, Mathur discloses the switch fabric interface communicates crossbar data (i.e. data transmitted between routing components (co. 7, lines 10-25).

9. Referring to claim 7, Mathur discloses the routing component is implemented using an ASIC (it is understood in the art and in the specification as defined on page 4, an ASIC is a circuit board or chip which is designed for a particular function, in this case the routing component 12 is integrated on a single switch chip, therefore it is implemented as an Application Specific IC, the Application in this case is to provide routing function) (Figure 2; col. 3, lines 55-60).

10. Referring to claim 8, Mathur discloses the embedded memory comprises a RAM (i.e. DRAM) (Figure 2, ref. 20).

11. Claims 9, 11-33, and 34-35 are rejected for similar reasons as stated above. Furthermore Mathur discloses comprising a second router having an embedded memory to store data communicated using the second network interface (col. 6, lines 3-10).

Response to Arguments

12. Applicant's arguments with respect to claims 1-9, and 11-35 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph E. Avellino whose telephone number is (571) 272-3905. The examiner can normally be reached on Monday-Friday 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A. Wiley can be reached on (571) 272-3923. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JEA
May 16, 2005

WILLIAM C. VAUGHN, JR.
PRIMARY EXAMINER